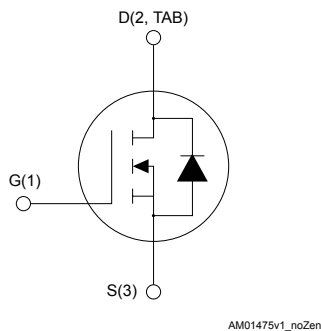
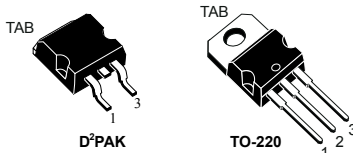



Automotive-grade N-channel 60 V, 32 mΩ typ., 30 A STripFET II Power MOSFET in a D²PAK and TO-220 packages



Features

Order codes	V _{DS}	R _{DS(on)} max.	I _D
STB36NF06LT4	60 V	40 mΩ	30 A
STP36NF06L	60 V	40 mΩ	30 A

- AEC-Q101 qualified 
- Exceptional dv/dt capability
- 100% avalanche tested
- Low gate charge

Applications

- Switching applications

Description

This Power MOSFET has been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.



Product status links

[STB36NF06L](#)
[STP36NF06L](#)

Product summary

Order code	STB36NF06LT4
Marking	B36NF06
Package	D ² PAK
Packing	Tape and reel
Order code	STP36NF06L
Marking	P36NF06L
Package	TO-220
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0\text{ V}$)	60	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20\text{ k}\Omega$)	60	V
V_{GS}	Gate-source voltage	± 18	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	30	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	21	
$I_{DM}^{(1)}$	Drain current (pulsed)	120	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	70	W
	Derating factor	0.47	W/ $^\circ\text{C}$
$dv/dt^{(2)}$	Peak diode recovery voltage slope	10	V/ns
$E_{AS}^{(3)}$	Single-pulse avalanche energy	225	mJ
T_{stg}	Storage temperature range	-55 to 175	$^\circ\text{C}$
T_J	Operating junction temperature range		$^\circ\text{C}$

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 30\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq T_J\text{ max}$.
3. Starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = 15\text{ A}$, $V_{DD} = 30\text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	2.14	$^\circ\text{C}/\text{W}$
R_{thJA}	Thermal resistance, junction-to-ambient	62.5	$^\circ\text{C}/\text{W}$
T_I	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified.

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	60			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 60\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 60\text{ V}$, $T_C = 125\text{ °C}$			10	
I_{GSS}	Gate body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 18\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1.0		2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 15\text{ A}$		32	40	m Ω
		$V_{GS} = 5\text{ V}$, $I_D = 15\text{ A}$		45	50	

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs}	Forward transconductance	$V_{DS} = 15\text{ V}$, $I_D = 15\text{ A}$	-	15		S
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	660		pF
C_{oss}	Output capacitance		-	170		pF
C_{rss}	Reverse transfer capacitance		-	70		pF
Q_g	Total gate charge	$V_{DD} = 30\text{ V}$, $I_D = 30\text{ A}$, $V_{GS} = 5\text{ V}$ (see Figure 13. Test circuit for gate charge behavior)	-	13	17	nC
Q_{gs}	Gate-source charge		-	4.2		nC
Q_{gd}	Gate-drain charge		-	7.8		nC

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 30\text{ V}$, $I_D = 15\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 5\text{ V}$	-	10	-	ns
t_r	Rise time		-	80	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	19	-	ns
t_f	Fall time		-	13	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		30	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		120	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 24 \text{ A}, V_{GS} = 0 \text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 20 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s},$	-	55		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 20 \text{ V}, T_J = 150 \text{ }^\circ\text{C}$	-	107		nC
I_{RRM}	Reverse recovery current	(see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	3.9		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

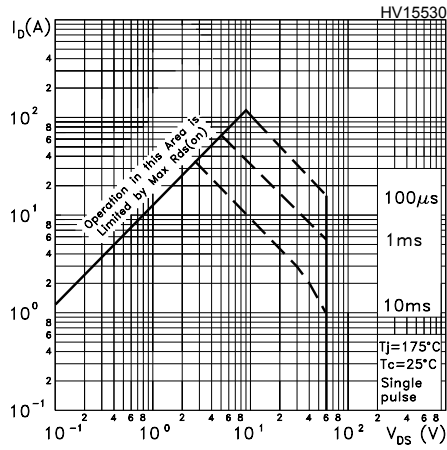


Figure 2. Thermal impedance

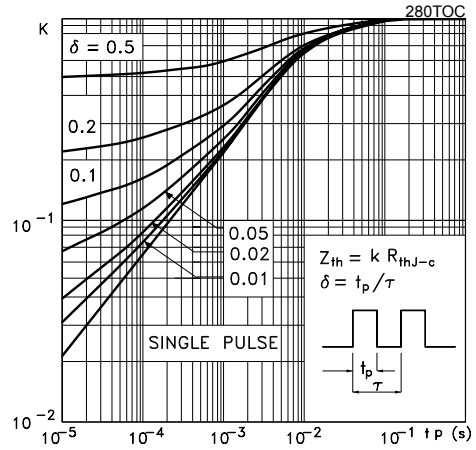


Figure 3. Output characteristics

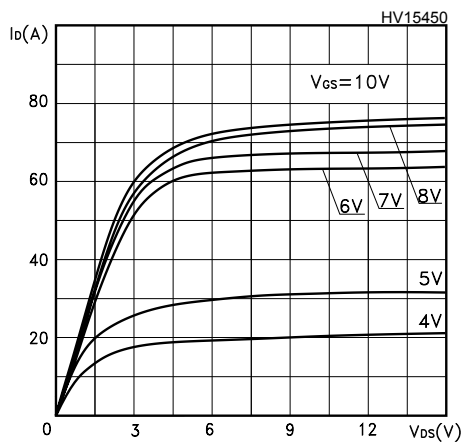


Figure 4. Transfer characteristics

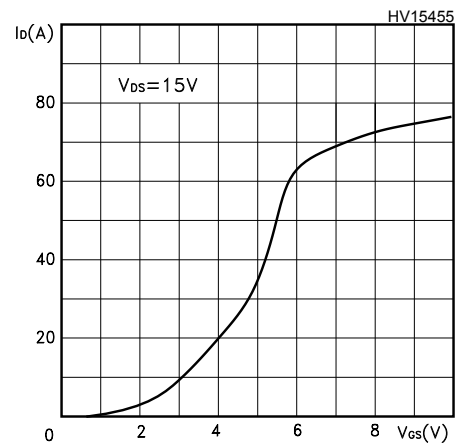


Figure 5. Transconductance

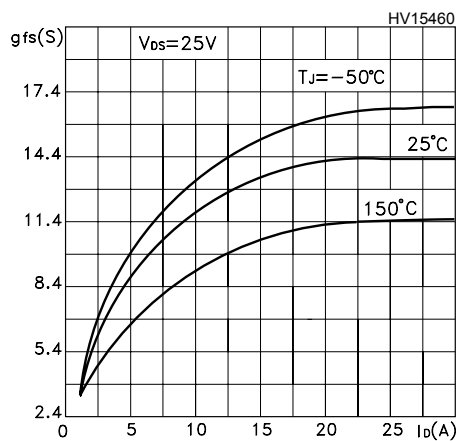


Figure 6. Static drain-source on-resistance

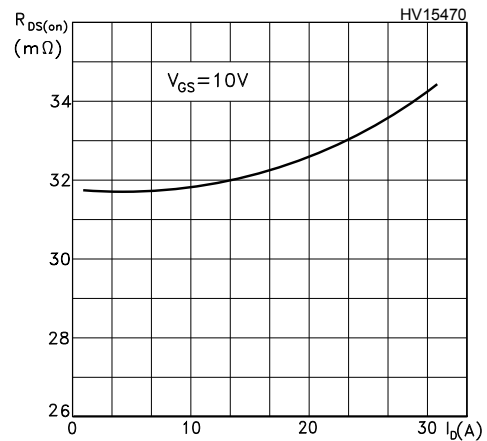
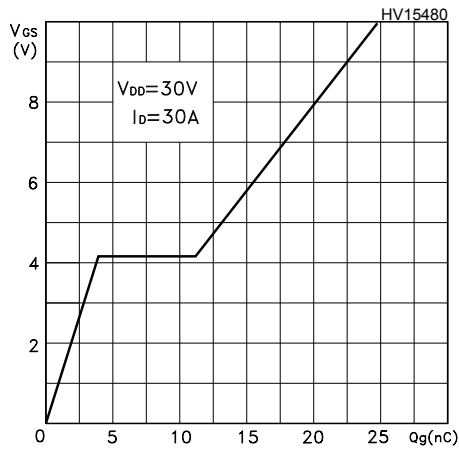
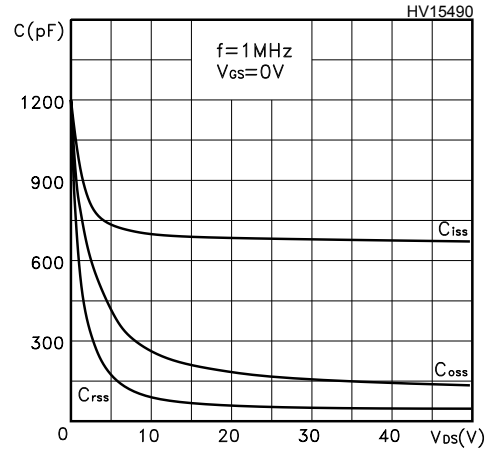
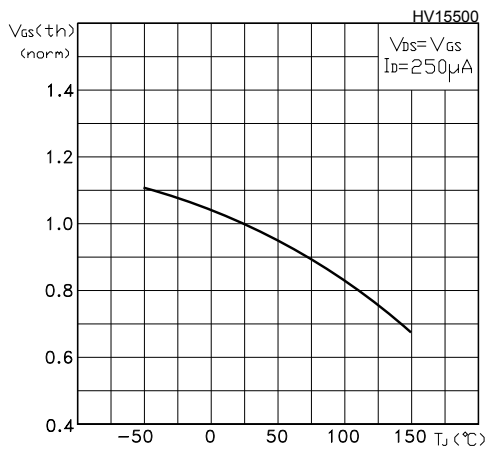
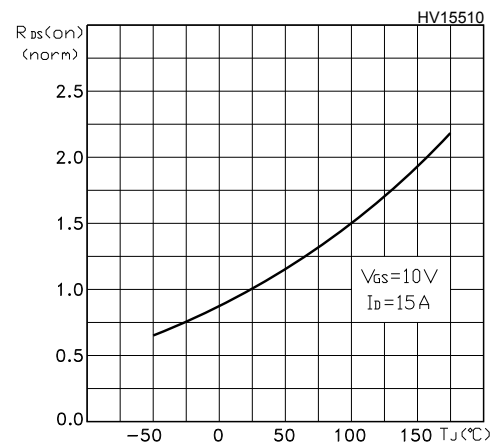
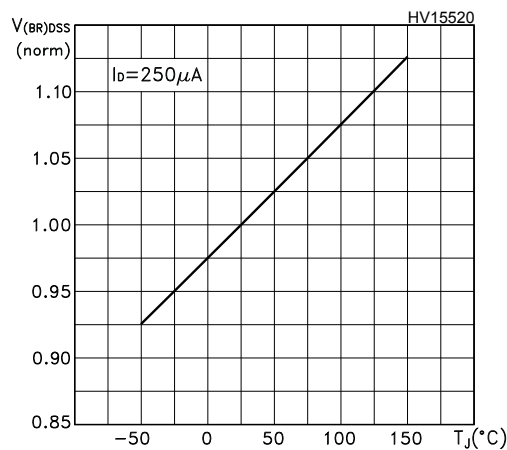
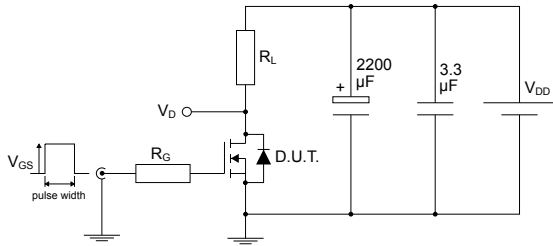
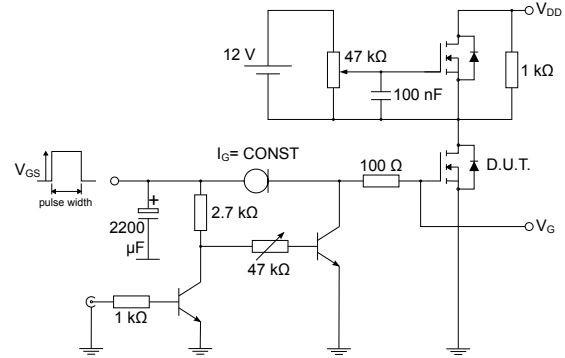


Figure 7. Gate charge vs gate-source voltage

Figure 8. Capacitance variations

Figure 9. Normalized gate threshold voltage vs temperature

Figure 10. Normalized on-resistance vs temperature

Figure 11. Normalized $V_{(BR)DSS}$ vs temperature


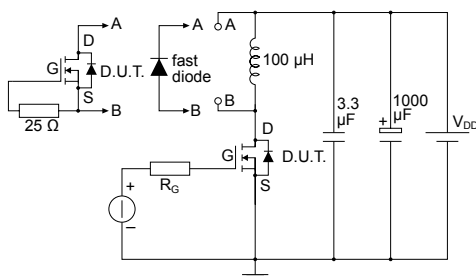
3 Test circuits

Figure 12. Test circuit for resistive load switching times


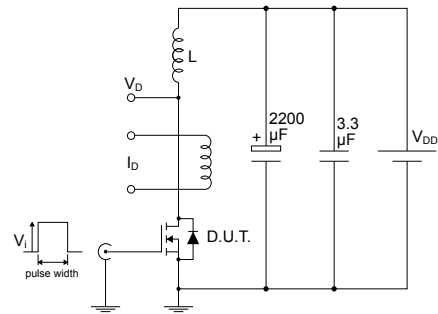
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Figure 13. Test circuit for gate charge behavior


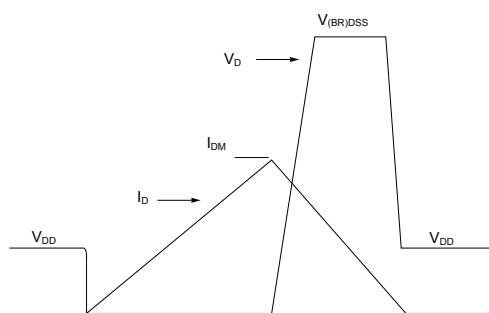
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Figure 14. Test circuit for inductive load switching and diode recovery times


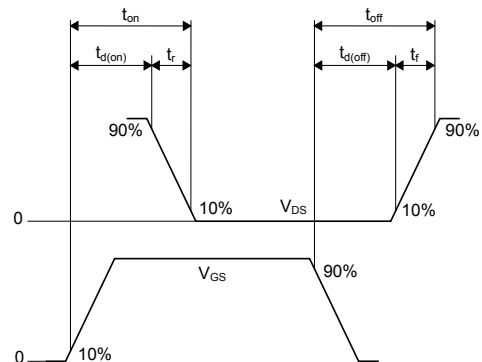
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Figure 15. Unclamped inductive load test circuit


AM01471v1

Figure 16. Unclamped inductive waveform


AM01472v1

Figure 17. Switching time waveform


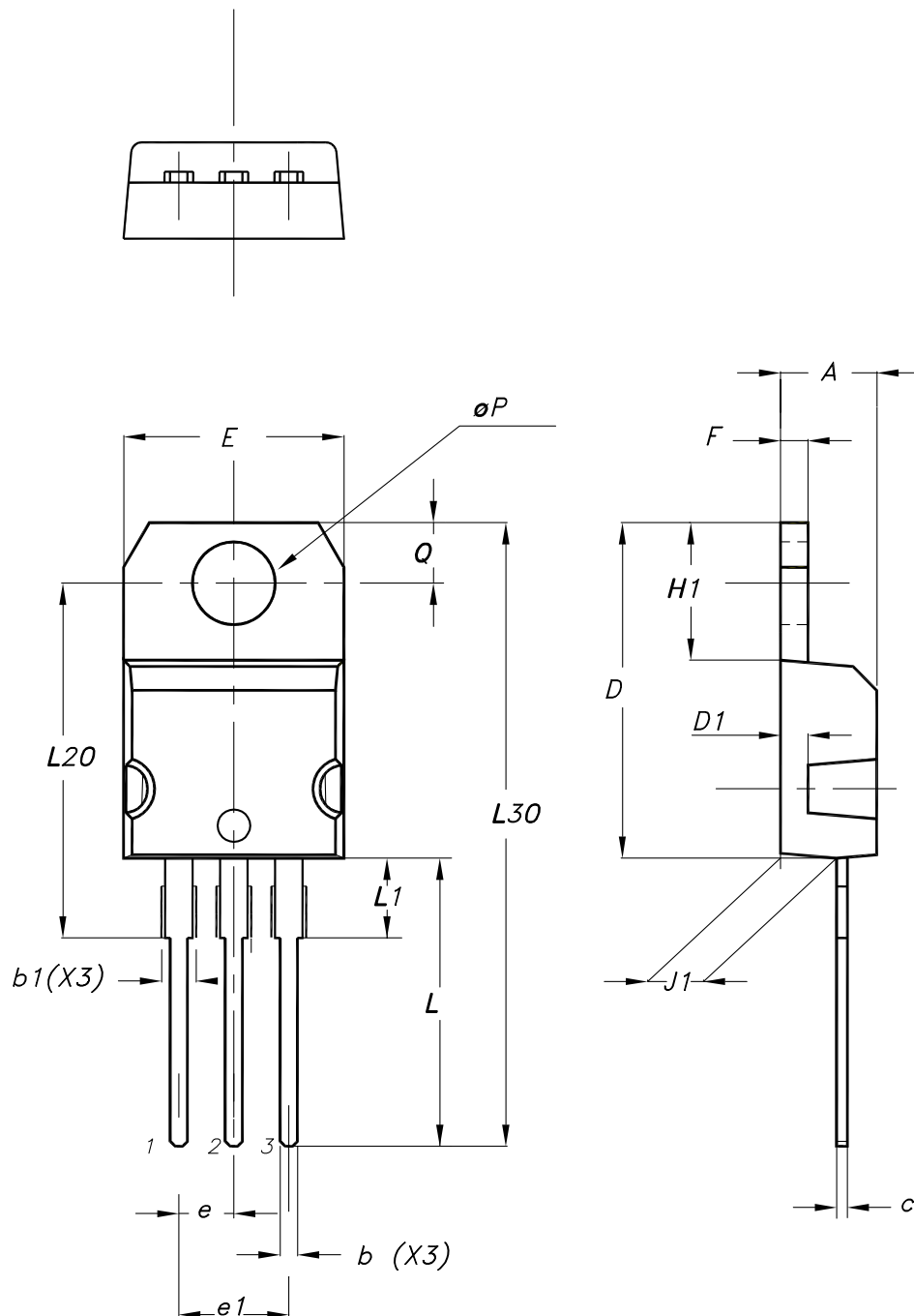
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220 type A package information

Figure 18. TO-220 type A package outline



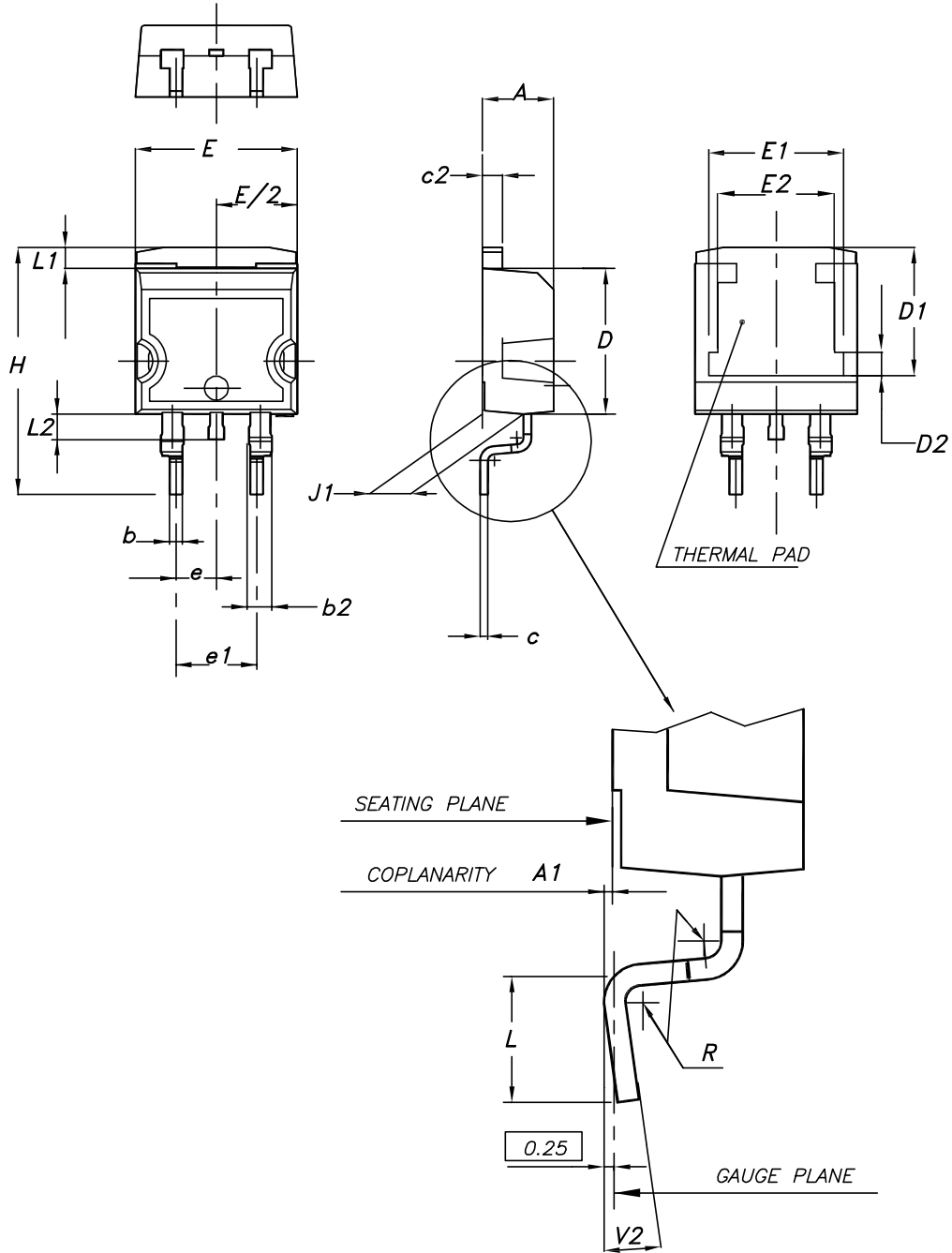
0015988_typeA_Rev_23

Table 7. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

4.2 D²PAK (TO-263) type A package information

Figure 19. D²PAK (TO-263) type A package outline

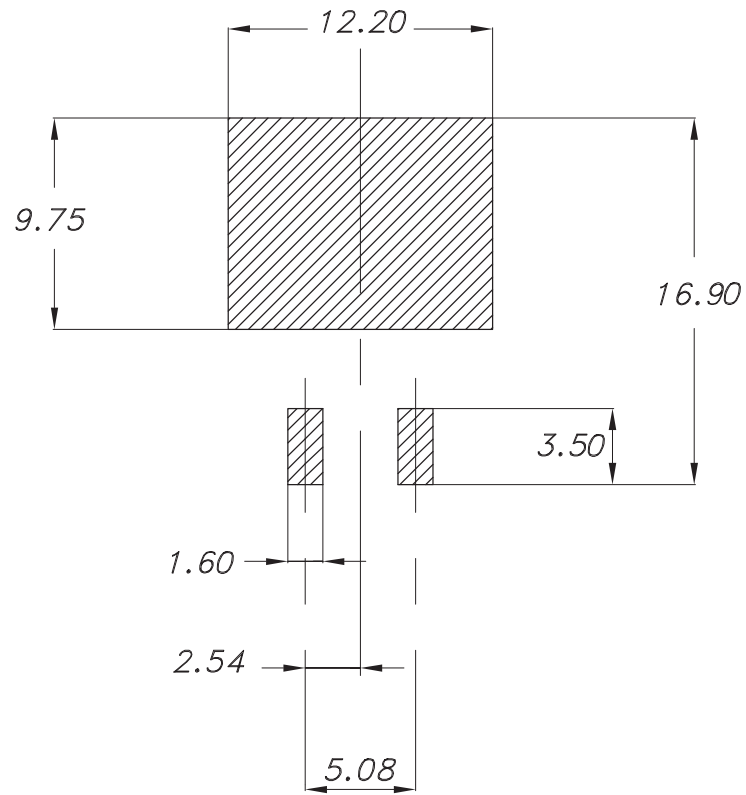


0079457_26

Table 8. D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

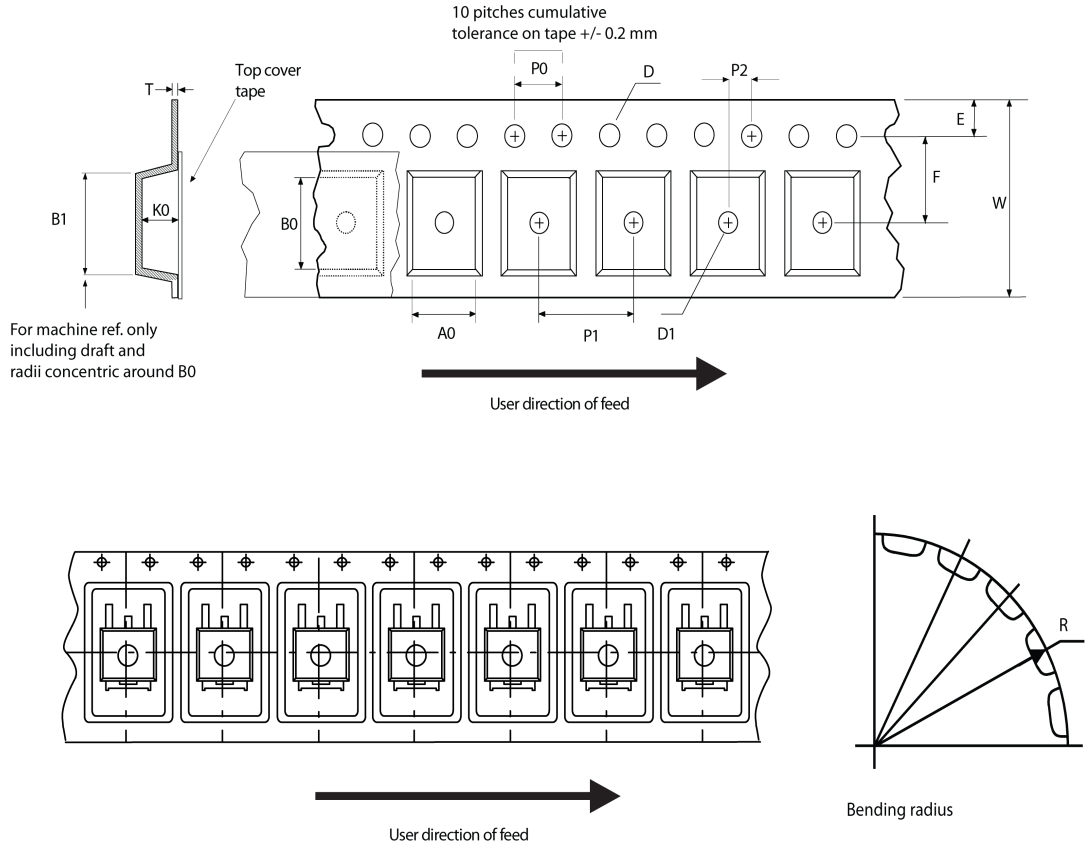
Figure 20. D²PAK (TO-263) recommended footprint (dimensions are in mm)



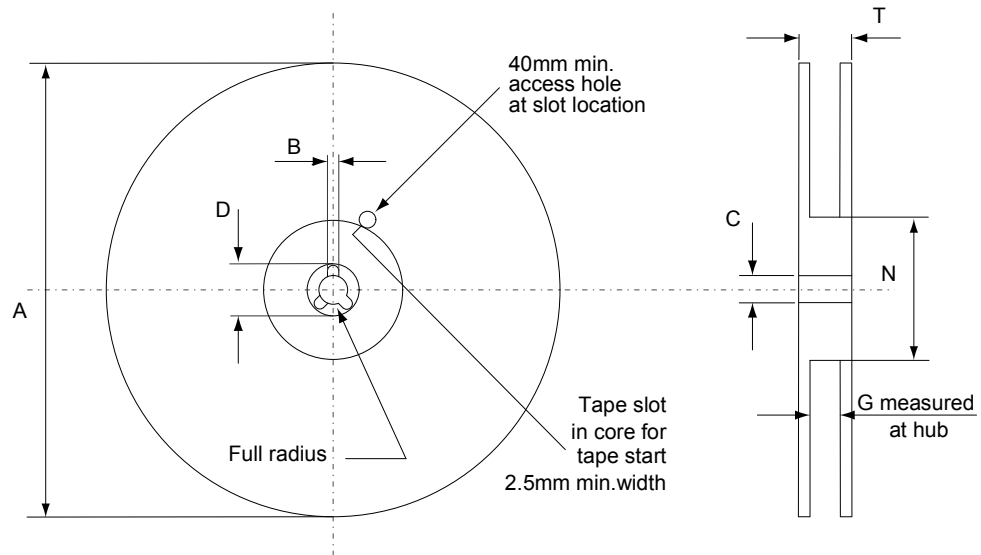
0079457_Rev26_footprint

4.3 D²PAK packing information

Figure 21. D²PAK tape outline



AM08852v1

Figure 22. D²PAK reel outline


AM06038v1

Table 9. D²PAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Revision history

Table 10. Document revision history

Date	Version	Changes
14-Jun-2003	1	First release.
13-Mar-2006	2	Complete version.
26-Jun-2006	3	New template, no content change.
07-Oct-2022	4	Updated title, Internal schematic , Device summary , Features and Description on cover page. Updated Section 4 Package information . Minor text changes.

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